A Designer's Guide

to Serial Transmitter and Receiver Measurements

Tektronix

Enabling Innovation

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Section 1: The Serial Data Revolution

In the beginning, digital systems relied almost exclusively on parallel transmission architectures. Each bit in a binary word had its own signal path from source to destination; its own transmitter, receiver, printed circuit board (PCB) trace, and termination.

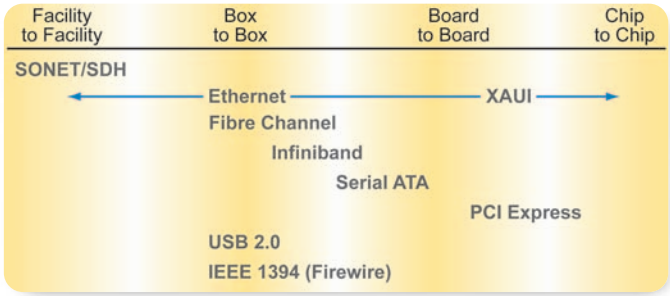
It was an elementary but workable topology. It took computing architectures from their earliest four-bit implementations to eight and sixteen bits; from clock rates of just a few MHz to almost a GHz. Parallel architecture is easy to understand, design, and troubleshoot.

But parallel techniques have their limitations, and these show up ever more clearly as data rates accelerate and word widths reach 32 bits and beyond:

– **Physical space limitations.** Even with the tiniest trace widths and spacings, a bus consisting of 32 traces (or more) consumes space needed for active components, connectors, etc. Making the PCB board larger is rarely an option.

– **Layout issues.** Aside from pure considerations of space, routing a wide parallel bus around a PCB inevitably requires dodging around components and other traces, frequent use of vias (through-holes), and splitting the bus to fit narrow passages. While computer-aided design techniques can simplify these processes, it remains difficult to avoid problems related to path length. Two presumably parallel bits will not arrive at the same time if they follow paths of differing lengths.

– **Bandwidth concerns.** As the data rate increases, even the small variations in delay within active devices – transmitters, buffers, etc. – can add up to a significant share of the unit interval (UI). In a parallel system, more transmitters mean more potential delay variations.



▶ **Figure 1.** *Serial data standards and application areas.*

– **Signal integrity implications.** Paths that have been closely spaced to save PCB space are prone to crosstalk. Vias, necessary to route signal traces past components and other features, can cause aberrations in the signal. PCB traces slimmed down to conserve real estate add inductance and delay to the signal path. Stray capacitance tends to increase as well. Ultimately, signal integrity suffers when wide parallel buses meet high data rates.

Serial Architectures Take the Lead In Computing Applications

With parallel bus technologies fast running out of room for bandwidth growth, system architects have turned to serial topologies. Today most emerging transmission solutions are serial in nature, sometimes with multiple "lanes" of serial data running simultaneously. The serial approach has found its way into many different applications and technologies, among which are those summarized in Figure 1. Most of these prominent serial applications relate to computer input and output (I/O) functionality at various system levels. In addition, several emerging multimedia standards have also adopted serial techniques. We will be discussing all of these applications[1] in more detail.

[1] SONET/SDH communication standards, although they are serial architectures, are beyond the scope of this primer.

Overview of Serial Computing Technologies and Applications

Ethernet

Ethernet is an external interface that is ubiquitous in computing networks around the world. It is the essential medium for connecting personal computers to local area networks (LAN) and to each other. It is a serial architecture that can utilize coaxial, CAT-5, or optical interconnect hardware.

Ethernet data rates have evolved from 10 Mb/s (still widely installed) to 100 Mb/s, and 1000 Mb/s (Gigabit Ethernet), with a 10 Gb/s technology known as 10 Gigabit Ethernet emerging today.

XAUI (10 Gigabit Attachment Unit Interface)

XAUI is an emerging technology that improves and simplifies the routing of electrical connections in chip-to-chip, board-to-board, and chip-to-optics module applications within digital systems. XAUI is a serial architecture that provides a composite data rate of 10 Gb/s via four differential signal pairs in each direction. XAUI has its origins in Ethernet technology. It is a subset of the IEEE 802.3ae standard for 10 Gigabit Ethernet architectures. XAUI is fast becoming the bus of choice for 10G Ethernet Z-Axis Pluggable Modules such as XGP and XENPAK. In conjunction with 10 Gb Ethernet, XAUI will enable very high-bandwidth connections from the computer's innermost components to the outside world.

FibreChannel

FibreChannel is a fast serial bus designed for high-speed enterprise networking applications. FibreChannel enables concurrent communication among workstations, mainframes, servers, storage area networks (SAN), and peripherals via established SCSI and IP protocols. It combines high-speed I/O and networking functions into an integrated connectivity technology. FibreChannel operates at distances of up to 10 kilometers.

Initially limited to 1 Gb/s data rates, FibreChannel has evolved into a fabric-switched architecture. Today's third-generation FibreChannel provides rates up to 2 Gb/s with the potential for 4 Gb/s rates in the future. FibreChannel is defined in a set of open standards developed by the American National Standards Institute (ANSI). Here the term "fibre" is taken to mean either copper or fiber-optic cabling, and the standard encompasses both media.

Infiniband

A serial architecture that is touted as a successor to FibreChannel in SAN applications, and as the transmission medium of choice for dense server blade installations and data centers. Infiniband eliminates the costly hardware adapters that some other technologies require, providing an efficient way to connect storage and communications networks and server clusters together to support an I/O infrastructure with superior reliability and scalability, as well as interoperability with other interconnect standards.

InfiniBand serial connections are created with links that rely on both copper wire and fiber optics for transmission. The Infiniband base data rate is 2.5 Gb/s. The standard promulgated by the Infiniband Trade Association also defines "4X and "12X" multipliers (using multiple lanes of communication) that yield effective data rates as high as 30 Gb/s. The trade association has announced plans to evolve Infiniband performance "beyond the 100 Gb/s barrier."

Serial ATA/Serial ATA Gen I and II

Serial ATA (SATA) was designed to succeed parallel ATA as the dominant interface connecting the CPU to hard disk drives within the PC. There is also provision to support other ATA and ATAPI devices, including CDs, DVDs, tapes devices, high capacity removable devices, zip drives, and CD-RW components. The highly scalable technology delivers a data bandwidth of 1.5 Gb/s to each drive connected to the bus. Aside from its throughput benefits, SATA fosters the use of smaller cables and connectors, enabling smaller PC enclosures and improving airflow. Consistent with digital system trends across the industry, SATA operates at lower voltages than its predecessor.

First-generation Serial ATA design goals specify a 1.5 Gb/s data rate, equivalent to 150 megabytes per second. The SATA Gen II Electrical Specification (July, 2004) defines a 3.0 Gb/s evolution and future plans envision a 6.0 Gb/s version of Serial ATA.

PCI Express

PCI and PCI-X are parallel interconnect architectures developed to allow PC makers and end users to easily connect peripheral components within a personal computer These might range from communication and storage I/O cards to consumer-grade audio cards. PCI Express is the high-speed successor to this very successful bus concept.

PCI-Express is a serial point-to-point interconnect that uses differential signaling. The serial interconnect scheme delivers high bandwidth over a small number pins, in contrast to the cumbersome 64-bit parallel transmission paths of earlier PCI variants. The "Generation 1" PCI-Express signaling data rate is 2.5 Gb/s in each direction, with rates up to 10 Gb/s planned. In addition, bandwidth can be proportionally scaled using multiple lanes.

PCI-Express will be cited in examples throughout this document, since it is a widely-used standard that exhibits "typical" serial device behavior.

Multimedia Serial Interfaces

All of the foregoing technologies are oriented toward computer I/O applications. Serial architecture has also found a home in some important serial multimedia interfaces. Following is a brief introduction to these interfaces; the topic is covered in more detail in Appendix A.

DVI (Digital Visual Interface)

DVI is a video interface technology designed specifically to support flat panel LCD monitors and high-end video graphics cards in the PC environment. It is intended to eliminate the digital-to-analog conversion that until now has been necessary to transmit data to a display device. DVI is also gaining ground as the preferred digital link for HDTV, EDTV, Plasma Display, and other high-end consumer video display media.

DVI is an external serial interface that uses transition minimized differential signaling (TMDS®) to convey information among system elements.

HDMI (High Definition Multimedia Interface)

HDMI is an uncompressed all-digital audio/video interface aimed primarily at consumer entertainment applications. HDMI provides an interface between audio/video sources (set-top boxes, DVD players, and A/V receivers) and audio and/or video monitor such as a digital television (DTV) component. HDMI supports standard, enhanced, and high-definition video as well as eight-channel digital audio.

HDMI uses the existing Digital Video Interface (DVI) architecture and adds capability for High Definition Audio and High-Bandwidth Digital Content Protection (HDCP). The latter technology enables true copy protection of high-quality digital movie content. HDCP is receiving an enthusiastic response from the entertainment industry, which is advocating its use in all HD consumer products.

Features And Characteristics Of Serial Transmission

In a basic serial architecture, binary words of 16, 32, or 64 bits or more are delivered sequentially along one path, whereas a parallel architecture distributes the word width among many paths. But serial devices differ from their parallel predecessors in other important ways. There are several key characteristics that have become almost universal in serial implementations: differential transmission, low voltage signaling, embedded clocks and 8B/10B Encoding. Most serial standards specify these attributes, which are essential to achieving data rates of 2.5 Gb/s, 5 Gb/s, 10 Gb/s, and beyond.

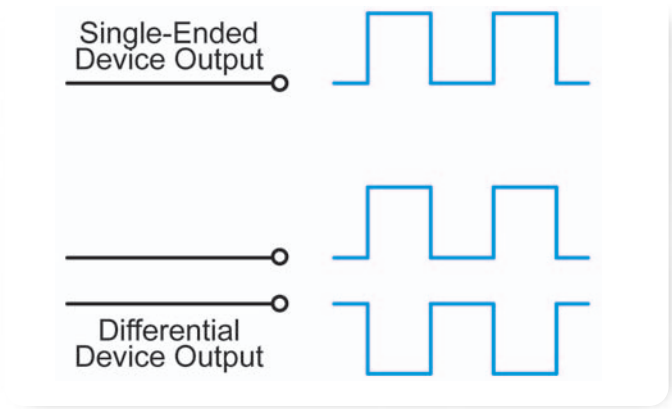
Differential Transmission

Differential transmission has been a part of communications technology since the early days of telephone networks. A differentially-transmitted signal consists of two equal and opposite versions of the waveform traveling down two conductors to a differential receiver[2]. When the signal on one leg of the differential path is going positive, the signal on the other leg is going equally negative, as shown in Figure 2. These two mirror images of the signal combine at the destination. Differential techniques resist crosstalk, externally-induced noise, and other degradations. Properly designed and terminated, a differential architecture provides a robust path for sensitive high-frequency signals.

Low Voltage Signaling

Increasingly, serial architectures that employ differential transmission also use low-voltage signaling. Not surprisingly, the approach is known as Low Voltage Differential Signaling, or LVDS. Fast buses often rely on very low-voltage signals simply because it takes less time to change states over the span of a few hundred millivolts, for example, than it takes to make a full one-volt transition. Outwardly this might seem more susceptible to interference and noise, but differential transmission protects against such effects.

A technique known as de-emphasis modifies certain bits in a given sequence. According to one established serial standard "…de-emphasis must be implemented when multiple bits of the same polarity are output in succession[3]." That is, the first bit following a series of bits having the opposite state is higher in amplitude than subsequent bits. These subsequent bits, then, are de-emphasized. The purpose of this practice is to counteract losses in transmission media such as FR4 circuit boards.



▶ **Figure 2.** *Single-ended vs. differential signals.*

Embedded Clocks

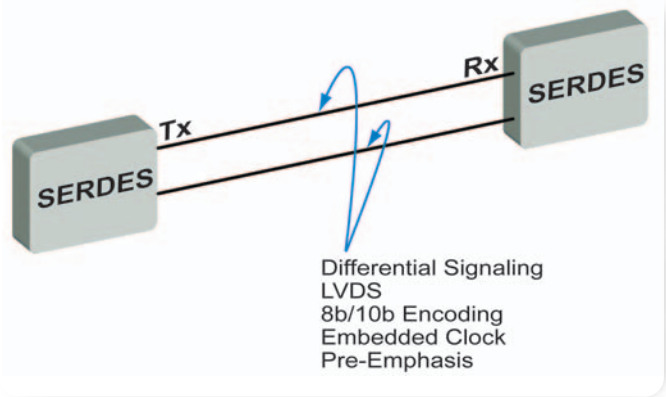
Many (if not most) current serial devices rely on embedded clock signals to maintain synchronization between transmitting and receiving elements. There is no separate clock signal line; instead, the timing information resides in the data signal. As we will see later in this document, this imposes certain requirements on the data signal. Encoding methods such as 8B/10B are used to guarantee that usable reference edges occur regularly enough to provide the needed synchronization.

8B/10B Signal Encoding

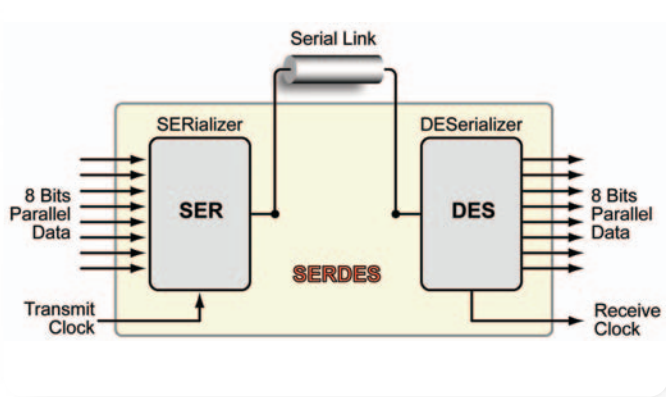
Many serial standards employ 8B/10B encoding, an IBM-patented technology used to convert 8-bit data bytes into 10-bit Transmission Characters. These Transmission Characters improve the physical signal to bring about several key benefits: bit synchronization is more easily achieved; the design of receivers and transmitters is simplified; error detection is improved; and control characters (such as the Special Character) can be more readily distinguished from data characters.

[2] Note: a single-ended signal sends only one instance of the signal, usually referenced to ground, to the receiving element.

[3] PCI Express Base Specification 1.0a



▶ **Figure 3.** *Transmission characteristics of a serial architecture.*



▶ **Figure 4.** *Typical SERDES architecture.*

The Building Blocks of Serial Architecture

A typical serial data configuration includes the transmitter and receiver components shown in Figure 3.

The Serializer/Deserializer (SERDES, Figure 4) is one of the fundamental building blocks this serial architecture. Essentially the SERDES is a component that integrates two key functions, supporting both transmission and reception of serial data.

The Serializer (SER) takes parallel data and converts it into a serial bit stream. The input is typically 8-bit parallel data which can be encoded with an optional 8B/10B encoder. This encoding scheme converts the 8 bits data into a 10 bit format that is transmitted over a serial output link.

The deserializer (DES) performs the reverse process. It takes the serial data, decodes and converts it back to parallel data, and delivers the result to a parallel interface along a clock signal recovered from the data.

Within the SERDES there are two primary functional elements. The first is a phase locked loop (PLL) clock recovery and multiplication block that takes a system reference clock and multiplies it up to the data bit rate. This element also recovers the embedded the clock from the data.

The second element is a sampler that uses the multiplied clock as a reference against which to latch the incoming serial data.

Section 2: Serial Measurement Overview

With the trend toward serializing computer I/O, serial data components, cables and connectors have become big business—a major investment for many high-technology companies, and a source of revenue for others. To guarantee interoperability among all these serial elements, detailed standards have been written to specify the interface characteristics and the tests required to verify them. In this primer we will concentrate on the Physical Layer (Electrical) specifications for the various standards.

As we saw earlier in this primer, serial data methods arose from the need to transfer data at faster rates. In parallel systems the requirement for synchronized clocks was the most difficult challenge. Due to timing skews related to edge speeds, keeping synchronizing the clock edges with the data as it traversed cables, connectors, and circuit boards traces was both challenging and expensive.

One of the earliest serial data standards was FibreChannel (FC). Many of today's standards use the testing concepts developed for FibreChannel. FC developers worked closely with the Technical Committee known as T11, a group formed to study the design and testing of future high-speed storage devices. Thanks to this collaboration, FibreChannel was among the first serial data standards to develop the embedded clock principal and to use LVDS designs. Many present-day serial specifications can trace their roots to the T11 committee.

	Inside the Box		Outside the Box						Display		Test Equipment			
Applications	PCI Express	Serial ATA II	Ethernet	Xaui	FibreChannel	InfiniBand	USB 2.0	IEEE1394B	DVI	HDMI				
Data Rate (max)	2.5Gb/s	3Gb/s	10Gb/s	3.125Gb/s	2.125Gb/s	2.5Gb/s	480Mb/s	1.6Gb/s	1.65Gb/s					
Lanes	up to 32	2 or 4	1	4	1	up to 12	1	1/63 nodes	3	3				
Encoding	8B10B	8B10B		8B10B	8B10B	8B10B	NRZI	8B10B	8B10B	8B10B				
Signaling	LVDS	LVDS		LVDS	LVDS	LVDS			TMDS	TMDS				
Embeded Clock	•	•		•	•	•					DTG	AWG	RT Scope	TDR/TDT
Reciever/Sink Tests														
Stressed Eye/Jitter Tolerance	•	•	•	•	•	•				•	•	•	•	
Receiver Sensitivity/Amplitude	•	•	•	•	•	•	•	•	•	•	•	•	•	
Timing Skew	•	•			•	•			•	•	•		•	
De-Emphasis	•		•	•	•	•					•		•	
PLL Loop BandWidth	•	•	•	•	•	•					•		•	
Transmiter/Source Tests														
Eye Diagram (Mask Testing)	•	•		•	•	•	•		•	•			•	
Transition Timing (Rise/Fall)	•	•		•	•	•	•		•	•			•	
Timing Skew	•	•		•	•	•			•	•			•	
Amplitude	•	•	•	•	•	•	•		•	•			•	
Common Mode	•	•	•		•	•							•	
De-Emphasis	•				•	•							•	
Jitter	•	•		•	•	•			•	•			•	
Return Loss			•									•	•	
Cable/Connector Tests														
Cross Talk	•	•			•	•				•	•		•	•
Transition Timing (Rise/Fall)	•	•			•	•				•				•
Loss	•	•		•	•	•	•			•	•	•		•
Impedance	•	•		•	•	•	•	•	•	•				•

▶ **Table 1.** *Compliance tests for serial data standards.*

Interoperability Is The Objective

Over time it has become clear that in order for an emerging standard to succeed in the market, specifications and testing criteria must be established early in its development phase to ensure interoperability.

At its heart, this document is about testing the parameters that support interoperability among elements complying with any given standard. We will focus on common specifications with general similarities across many serial standards. We will address such topics as LVDS; embedded clocks and clock data recovery; embedded SERDES (serializer/deserializer) devices; embedded transmitter (Tx) and receiver (Rx) sections; 8B/10B data encoding, and signal de-emphasis.

Serial bus compliance, interoperability, and troubleshooting measurements are divided into two categories— Receiver (Rx) and Transmitter (Tx). Rigorous receiver measurements require a high-bandwidth oscilloscope and a signal source—typically a data generator or arbitrary waveform generator. The latter instrument provides complex stimulus data and "stress" signals to the device.

Transmitter measurements require an oscilloscope, sometimes aided by other specialized acquisition hardware.

Some oscilloscopes can be equipped with integrated measurement applications. For example, the Tektronix TDS7000B Series offers optional packages such as TDSRT-Eye Serial Measurement software and TDSJIT3 v2.0 Jitter Measurement software. These tools can carry out complex setup, acquisition, analysis, and display steps automatically.

Table 1 summarizes today's prevailing serial data standards and their required compliance tests.

Receiver (Rx) Measurements

During Rx testing, data from a signal source drives the device under test while an oscilloscope monitors the output to ensure that the device will work at nominal and stressed levels. Rx specifications, like their Tx counterparts described in the following section, include three basic signal characteristics that must be verified: amplitude; timing; and jitter tolerance. In Rx testing, impedance characteristics may be included as well. Because the Rx section of the device must be interoperable with many device types connected through various interconnects, its specification is in many cases more challenging than that of the Tx section.

Most present-day serial devices, whether they function as "transmitters" or "receivers," actually employ SERDES components internally. This enables loopback testing and other techniques. In order to guarantee interoperability the Rx section has to be tested over a broad range of conditions, particularly in the Clock Data Recovery (CDR) and Deserializer components. Figure 5, the Rx section, illustrates the discussion that follows.

Incoming data reaching the receiver contains the embedded clock and is forwarded to the CDR. The CDR must be able to recover (extract) the clock while tolerating a range of amplitude and jitter conditions.

Similarly, the deserializer must be able to handle specified amplitude, jitter, and skew variations. Manufacturers developing these serial components often provide a way to insert test data (stimulus) streams that exercise the component in the manner prescribed by the applicable standard.

While the quantifiable test parameters and tolerances vary from one standard to the next, the basic test methodology can be summarized as follows:

– Put the device in a loopback mode

– Insert a test pattern

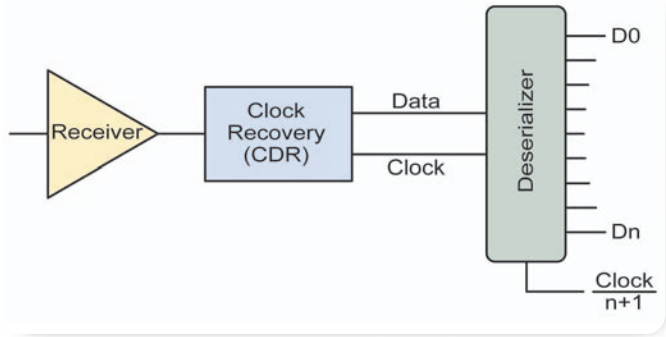
– Vary the amplitude for sensitivity testing

– Insert jitter to make sure the clock recovery PLL can track the input

– Vary the timing skew between differential pairs to allow for tolerances in board layout and cabling

Rx Amplitude Sensitivity Measurements:

For testing to standards such as PCI Express, Infiniband, and FibreChannel a programmable digital timing generator capable of producing data patterns is needed. The generator must be able to generate training packets or pseudo-random bit stream (PRBS) data that can be varied in amplitude. The generator must generate signals containing the de-emphasis characteristics or equalization used to compensate for signal loss in the transmission media. De-emphasis



▶ **Figure 5.** *Typical receiver block diagram (FibreChannel).*

must be applied when a succession of bits of the same polarity occurs. Bits following the first bit are driven at a voltage level 3.5 dB (+/-.5 dB) below the first bit (see Figure 9). The individual bits, including the first bit from a sequence in which all bits have the same polarity, must always fall between the Min and Max values specified by the VTX-DIFFp-p characteristic in Table 4-5 of the PCI Express Base specification.

Other standards such as Ethernet and SATA may additionally require an Arbitrary Waveform Generator (AWG) that can deliver both logic patterns and analog waveforms. The latter signals simulate the return loss characteristics of the device under test (DUT) and cables. Once these signals are applied to the Rx section the circuit can then be verified using techniques similar to those used in testing the Tx section. The goal is to verify that the training pattern is still correct, or that a predicted sequence or pattern has been established.

Rx Timing Measurements

These measurements deal with inserting delays or skewing the data between the differential pairs and data lanes. This ensures that the receiver can tolerate variations in circuit board traces and cable and connector components. Other tests require inserting specific patterns or training sequences to verify that the receiver can tolerate differences in edge transition or rise and fall rates.

Rx Jitter Tolerance Measurements

As serial data buses achieve faster data rates, jitter becomes one of the most difficult issues to resolve. To guarantee interoperability the CDR and SERDES must be able to tolerate a defined amount of jitter. Many papers and application notes have been written on this topic so we will discuss the details of this measurement specification only briefly.

In the case of FibreChannel devices, the Receiver jitter tolerance is a measure of how well the Clock and Data Recovery Unit (CDR) within the link receiver can tolerate jitter in its various forms. Two questions pertaining to CDR behavior are important.

First, how much horizontal eye closure can the CDR tolerate with its recovered bit clock strobe optimally placed in the eye? This result reflects how well the CDR centers its recovered bit strobe in the data eye. It also reveals the setup and hold times are for the CDR's input phase lock loop circuit.

Secondly, how much does the CDR's recovered bit clock wander as it attempts to track jitter within or below its passband frequency? The result is very much influenced by the jitter spectral components present in the serial data and the amount of system noise that is coupled to the CDR bandpass filters.

Note that any jitter tolerance property can be affected by other signal characteristics such as amplitude and rise time. In effect, jitter tolerance is a bit error ratio measurement: a bit sequence with a known amount of jitter is applied to the input and the receiver's resulting error ratio is measured. This procedure requires an error-detecting instrument in addition to a pattern source and jitter generator. Note that jitter tolerance measurements generally require long test times, since they must record literally trillions of cycles to ensure 10^{-12} bit error ratio performance. An oscilloscope with high capture rate and jitter analysis tools can reduce test times for these jitter tolerance tests.

Transmitter (Tx) Measurements

As explained earlier, the oscilloscope (DSO or DPO) is the centerpiece of serial transmitter measurements. Modern oscilloscopes can be equipped with probing tools, memory configurations, and application-specific measurement software optimized for fast, accurate serial measurement results.

Tx Amplitude Measurements

Amplitude measurements determine whether the signal achieves the voltage levels and stability needed to reliably pass through the transmission medium and communicate a proper "one" or "zero" to the receiving circuit. The tests ensure that the signal has enough amplitude tolerance to do its job under worst-case conditions.

- **Differential Voltage:** every serial specification has a peak-to-peak differential voltage specification. This is the fundamental specification guaranteeing that the device under test is transmitting the correct voltage levels. The minimum transmitter differential voltage is specified such that a stated minimum differential voltage will arrive at the receiver under worst-case media conditions (maximum loss). This ensures proper data transfer.
- **De-Emphasis:** this is the ratio of the amplitude of the second and subsequent bits after a "transition bit" to the amplitude of the transition bit itself. Related terms are pre-emphasis[4] and equalization. De-emphasis is used in serial data transmission systems to compensate for the frequency characteristics of "lossy" media such as the low-cost FR4 boards and connectors used in desktop computers. By making the transition bit higher in amplitude than the subsequent bits, the signal will arrive at the receiver pins with an "open eye."

[4] There is some ambiguity in industry documentation about the terms "de-emphasis." This Primer, following the example of the PCI Express base specification, will use the term "de-emphasis" to signal amplitudes denote deliberately reduced under specific conditions.

– **Common Mode Voltage Measurements (AC, DC):** common-mode imbalance and noise on the transmitter can create undesirable effects in the differential signal. It is often useful to break apart a differential signal into its single-ended components to troubleshoot such issues. This technique also pinpoints crosstalk and noise effects that may be coupling into one side of the differential pair and not the other.

– **Waveform Eye Height:** eye height is the data eye opening in the amplitude domain. This very useful measurement represents the actual sample point of the receiver circuit. It is measured at the .5 Unit Interval (UI) point, where the UI timing reference is defined by the recovered clock.

Tx Timing Measurements

Timing measurements are designed to confirm that the signal is free from timing variations, with transitions fast enough to preserve the critical data values the signal is meant to deliver. These tests, which require uncompromised performance on the part of the measurement toolset, detect aberrations and signal degradation that arise from distributed capacitance, crosstalk, and more.

– **Unit Interval and Bit Rate:** variations in the embedded clock frequency can be measured by looking at the mean measurement of the embedded clock over a large number of consecutive cycles. According to some standards, a mean measurement greater than 100 parts per million (PPM) away from the specified value is considered a DUT failure.

– **Rise/Fall Time:** even though risetimes that are too fast can cause EMI problems, while those that are too slow rise can cause data errors, some standards do not include rise time as part of the compliance test series. This is simply due to the measurement errors that can be introduced by the instrument (typically and oscilloscope) and its probes. However, by applying the "square root of the sum of the squares" formula to the measured value, it is possible to determine whether the driver is approaching a rise/fall time failure.

– **Waveform Eye Width –** waveform masks can be confusing when used to validate transmitter compliance. Section 6 of the Serial ATA specification says that the statistical certainty achieved by capturing a waveform and comparing it to a mask cannot guarantee compliance to the required 10^{-12} BER ($\pm 7\ \sigma$) standard.

This is due to the number of actual edges that can be captured in a reasonable amount of time. However, the waveform eye width is a good check for the health of the signal. It can serve as a simple "plugfest friendly" test as long as the number of edges required to support a statistical certainty is specified.

Waveform eye width should not to be confused with jitter eye width, which does provide statistical certainty down to 10^{-12} BER levels.

Tx Jitter Measurements

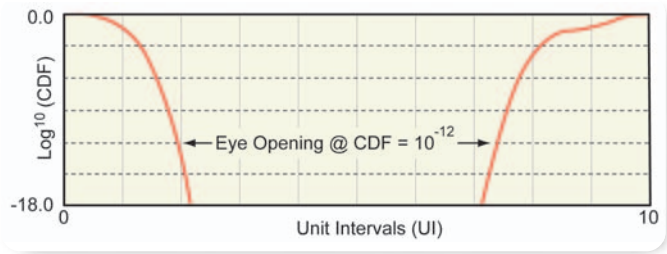
Jitter measurements are so important that specialized analysis tools exist to help designers penetrate this difficult problem. Time interval error (TIE) is the basis for many jitter measurements. TIE is the difference between the recovered clock (the jitter timing reference) and the actual waveform edge. Performing a histogram and spectrum analysis on a TIE waveform provides the basis for advanced jitter measurements.

At this writing there are few consistent jitter measurement methods, aside from eye diagrams, among published standards. In FibreChannel, InfiniBand, and XAUI, methods have been developed by the T11.2 jitter working group. "Methodologies for Jitter Specification" (MJS) published in 1999 defines total jitter as "the sum of random and deterministic jitter components." More recently, this work has been updated by the T11.2 in the form of "Methodologies for Jitter and Signal Quality Specification" (MJSQ).

The relationship to Total Jitter (TJ), Jitter Eye Opening (at 10^{-12} BER), and Unit Interval is as follows (Equation 1):

Total Jitter + Jitter Eye Opening = 1 Unit Interval

Equation 1: Jitter relationships



▶ **Figure 6.** *"Bathtub" curve or Cumulative Distribution Function.*

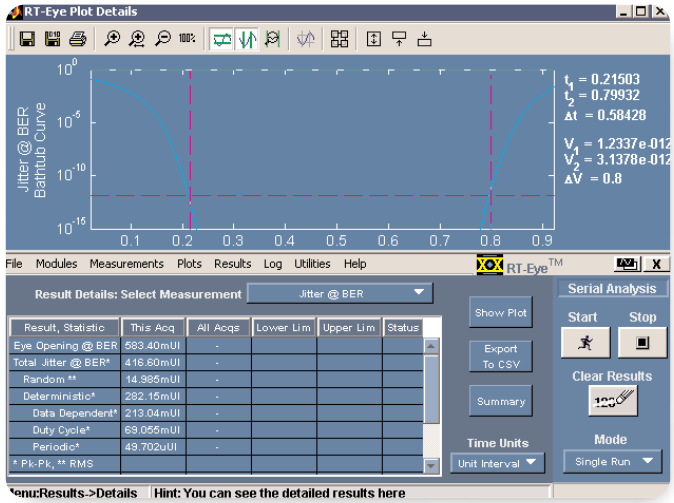
The first step in determining Total jitter is to establish a jitter timing reference using a "Golden PLL" model to recover the clock from the serial bit stream. The Golden PLL loop bandwidth is defined by fc/1667, where fc is the bit rate.

From the jitter timing reference, a Cumulative Distribution Function (CDF), also known as a "bathtub curve" (Figure 6) is established. This distribution reveals where the eye opening at 10^{-12} BER occurs.

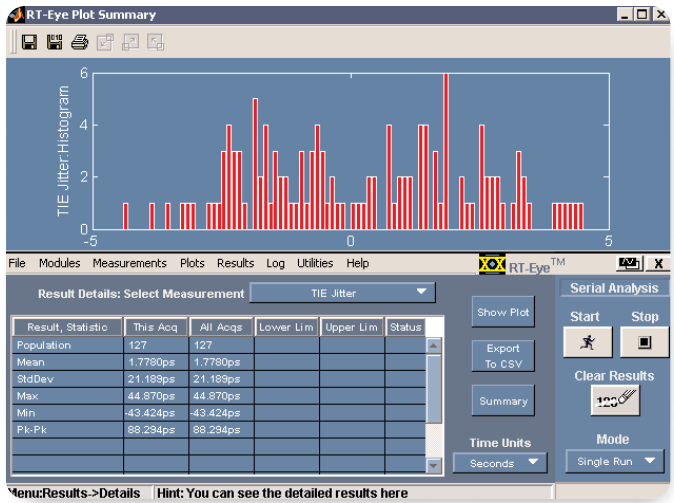
Traditionally these measurements have been cumbersome to make with the normal BERT or Time Interval Analyzer (TIA) instrumentation. Today there are automated jitter measurement software toolsets available for real-time oscilloscopes. These packages can establish the timing reference and the CDF, and then separate the Random and Deterministic Jitter (Rj/Dj) components in the signal.

Standards such as Serial ATA and PCI Express agree that the total jitter is the sum of random and deterministic components. However, various models for clock recovery exist. These standards call for the clock to be recovered from a set number of consecutive bits in the serial bit stream. These jitter methods are used because there is recognition that different forms of clock recovery such as oversampling or phase interpolation can be implemented. Figures 7 and 8 show two different jitter measurement methods used on the same 2.5 Gb/s signal.

In Figure 7, the Total Jitter and Deterministic Jitter (as specified in the InfiniBand standard) is shown. Total Jitter is determined using the bathtub curve method. In this case, the Jitter Eye opening is .583 UI and the Total Jitter is .417 UI at 10^{-12} BER.



▶ **Figure 7.** *Total jitter and deterministic jitter measurement determined using Infiniband compliance methodology.*



▶ **Figure 8.** *Results of a 250-cycle jitter test performed using PCI Express compliance methodology.*

Figure 8 shows the "250 Cycle Jitter" test specified in PCI Express. The Median to Max outlier is determined by the median of the TIE histogram to the maximum outlier on the histogram; in this case, 44.87 ps measured over any 250 consecutive bits. Figures 7 and 8 exemplify just two among several possible methods.

Tx Eye Diagrams and Mask Testing

The "eye diagram"—a waveform display consisting of many overlapping transitions—is an important tool for establishing the quality of serial signals. To produce an eye diagram, it is necessary to trigger the oscilloscope synchronously to the data stream and connect the input channel to the data stream carrying random or pseudorandom bits. A synchronous clock signal, the data itself or the clock recovered from the data (if the oscilloscope has a clock recovery circuit) triggers the oscilloscope. In one captured screen, all possible signal transitions of the signal are displayed: positive-going, negative going, leading, and trailing. This single display provides information about the eye opening, noise, jitter, rise and fall times, and amplitude. The display can be used for qualitative analysis, while the integrated statistical tools within the oscilloscope can make quantitative measurements. Rather than extracting numeric information on the signal characteristics, the two-dimensional eye shape can easily be compared to a group of violation zones called a mask.

In addition to the eye diagram analysis, more precisely quantified measurements may be required. For accurate jitter measurements an oscilloscope with jitter analysis tools is recommended. Impedance characteristics also must be measured. Time Domain Reflectometry (TDR) is a convenient way to evaluate impedance values and variations along a transmission line including cables, connectors or a microstrip on a PC board.

For more in-depth information on mask testing, refer to "The Basics of Serial Data Compliance and Validation Measurements[5]," a primer available through the Tektronix website. For details on impedance measurements, consult "TDR Impedance Measurements: A Foundation for Signal Integrity" an application note available from Tektronix.

Section 3

Serial Measurement Equipment and Methods

We have described in general the measurements required for the Rx and Tx elements of a serial device. This section will explain how to make these measurements using appropriate equipment.

Receiver Amplitude Sensitivity Measurements

The receiver amplitude sensitivity test is common to many serial standards. The test confirms that the receiver meets interoperability requirements even when it experiences attenuated or higher amplitude voltage swings. For example, the USB standard has a squelch measurement requiring the DUT to deliver a transmission envelope that does not indicate squelch (reliably receives packets) even when the packet's differential amplitude exceeds 150 mV or falls below 100 mV. The test procedure can be summarized as follows:

– Using a data timing generator or AWG, set the data pattern appropriately and adjust data packet the amplitude to the nominal value

– Decrease or increase amplitude until unit fails to respond correctly

– Verify amplitude is outside specification when the failures occur

[5] Publication 55W-16736-X, available at www.tektronix.com

Receiver Timing Skew Measurements

The Receiver device also must tolerate a certain amount of timing skew (misalignment) within respective data channels and differential pairs. Each specific standard defines a limit required for this skew tolerance.

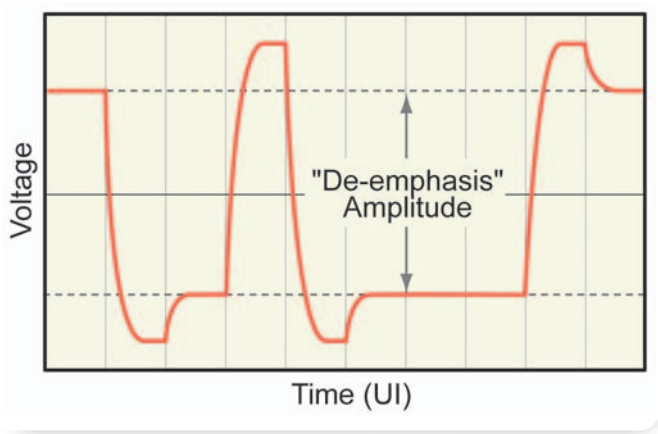
The test starts with the clock and data pairs to zero skew and then increases the skew until the device displays an error. The maximum skew setting that still provides error-free operation is defined as the tolerated skew; this result is compared against the published limit. If the skew tolerance is greater than the specified value, the device is considered compliant with the standard. The DTG5000 Series uses its unique differential timing offset capability in conjunction with two channels of a differential DTGM30 module to fulfill this test requirement.

Receiver PLL Loop Bandwidth Measurements

One common means of determining the PLL loop bandwidth is to use a jitter transfer function. This test characterizes the jitter amplitude response of the DUT as a function of jitter frequency. The test feeds the DUT a modulated reference clock signal (preferably with the modulation derived from a Gaussian noise source) and measures the jitter at the input and the output of the DUT. The ratio of the output jitter to the input jitter, plotted in the frequency domain, forms the transfer function plot and illustrates the loop bandwidth.

There are two expedient approaches to running the PLL loop bandwidth test:

– A DTG5000 Series instrument can do the job when equipped with a DTGM31 jitter module. An external Gaussian noise generator modulates the reference clock signal.

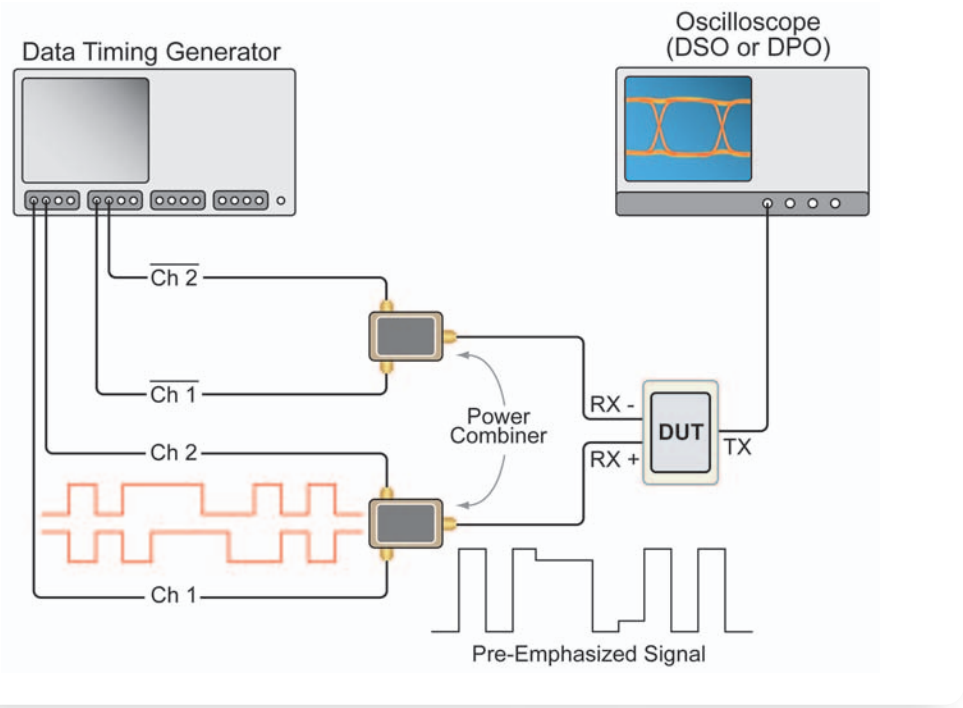


▶ **Figure 9.** *De-emphasis applied to a serial signal. The first bit following a series of bits of the opposite state is higher in amplitude than the "de-emphasized" bits that follow it. In this instance the amount of de-emphasis is -3.5 dB.*

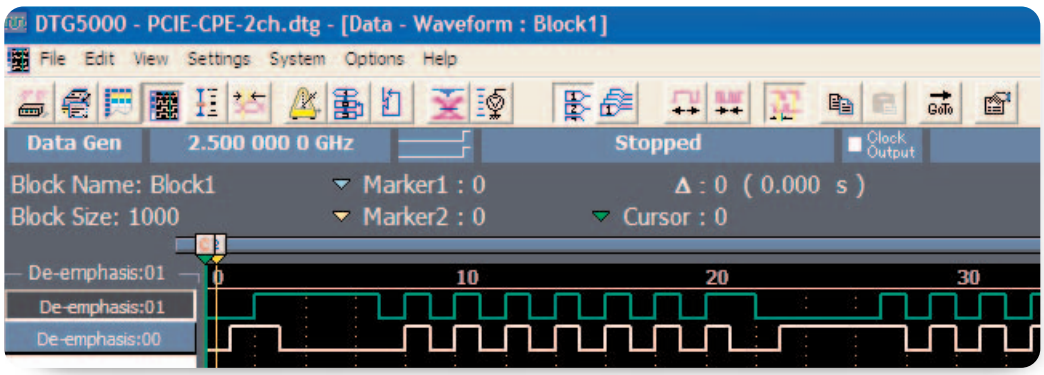
– An AWG615 or AWG710B's marker outputs, oversampled with a pseudo-random bit stream (PRBS) pattern, can be fed to the PLL. Using an oscilloscope running TDSJIT3 v2.0 jitter measurement software, the jitter value can be measured at the input and output of the PLL device and plotted.

Receiver De-Emphasis Generation and Testing

De-emphasis is required for many high-speed serializer/deserializer (SERDES) applications, and these characteristics play an important role in receiver testing. Figure 9 illustrates the concept in simplified form (only one side of the differential pair is shown). There are two logic voltage values, with a slightly higher voltage applied to any bit that follows a sequence of bits having one polarity (state).



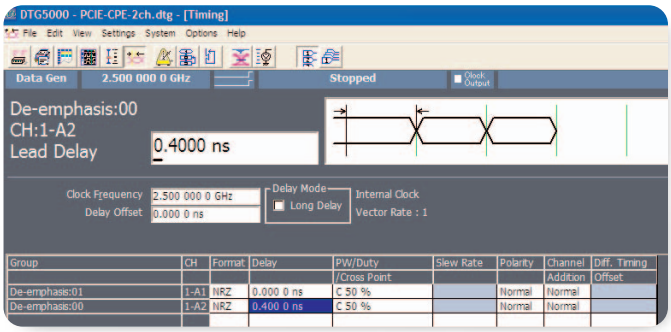
▶ **Figure 10.** *Creating the de-emphasis effect on a serial signal.*



▶ **Figure 11.** *Copying and pasting a duplicate waveform image.*

The stimulus source—in this case the data timing generator—must simulate de-emphasis in order to mimic the real-world conditions the SERDES will encounter. The de-emphasis tests require a pair of outputs from the DTG5274 Data Timing Generator driving a pair of power combiners as shown in Figure 10. If a suitable pre-written pattern exists, this may be loaded into the two channels of the data timing generator.

If a pre-written de-emphasis pattern is not available, it is easy to create the necessary data. Simply load the desired test pattern into the Channel 1 memory, then create a copy and paste the same image into the Channel 2 memory as shown in Figure 11 (Copy and Paste functions reside in the Waveform menu).



▶ **Figure 12.** *Inverting and delaying the waveform.*

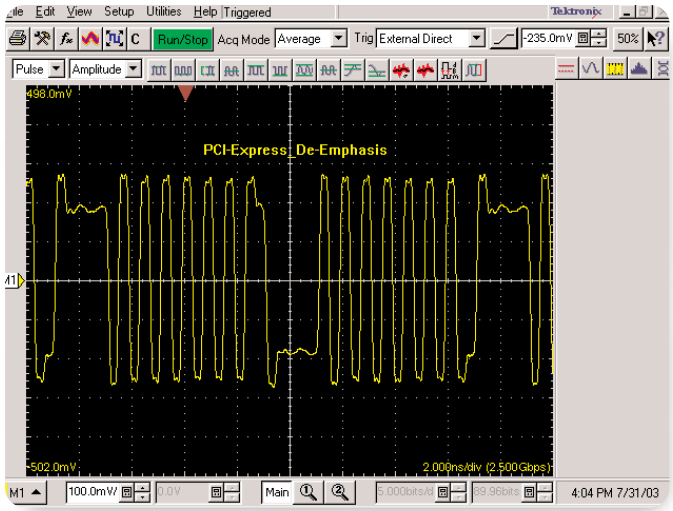
Using the Timing menu (Figure12), invert the Channel 2 signal and delay the clock by one unit interval (400ps).

Connect a power combiner from the DTGM30's Channel 1 and Channel outputs, and a second power combiner to those channels' complementary outputs. The resulting signal is a differential pattern with adjustable de-emphasis amplitude levels. Figure 13 is an oscilloscope view of such a signal. These levels can be set to accommodate losses incurred in the power combiners (usually 50%), and to vary the amounts de-emphasis during stress testing. Tools included in the software measure the actual de-emphasis value.

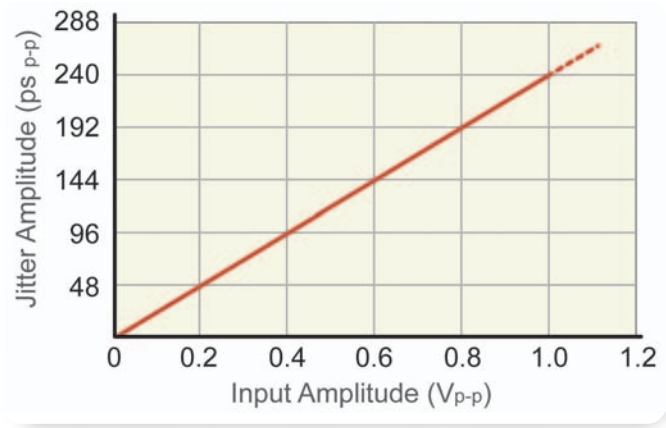
Signal jitter is one of the more difficult compliance issues confronting serial device designers. The best way to forestall jitter problems is to stress-test serial devices in advance with jitter that has known, controllable characteristics including amplitude and frequency. Successfully testing the devices under stressful jitter conditions is an avenue toward interoperability and end-user satisfaction.

Rx Jitter Tolerance Measurements

Jitter tolerance for receivers is defined as the ability to recover data successfully in the presence of jitter. Meeting the specification guarantees that the SERDES and PLL circuits can recover the clock even when a certain amount of jitter is present.

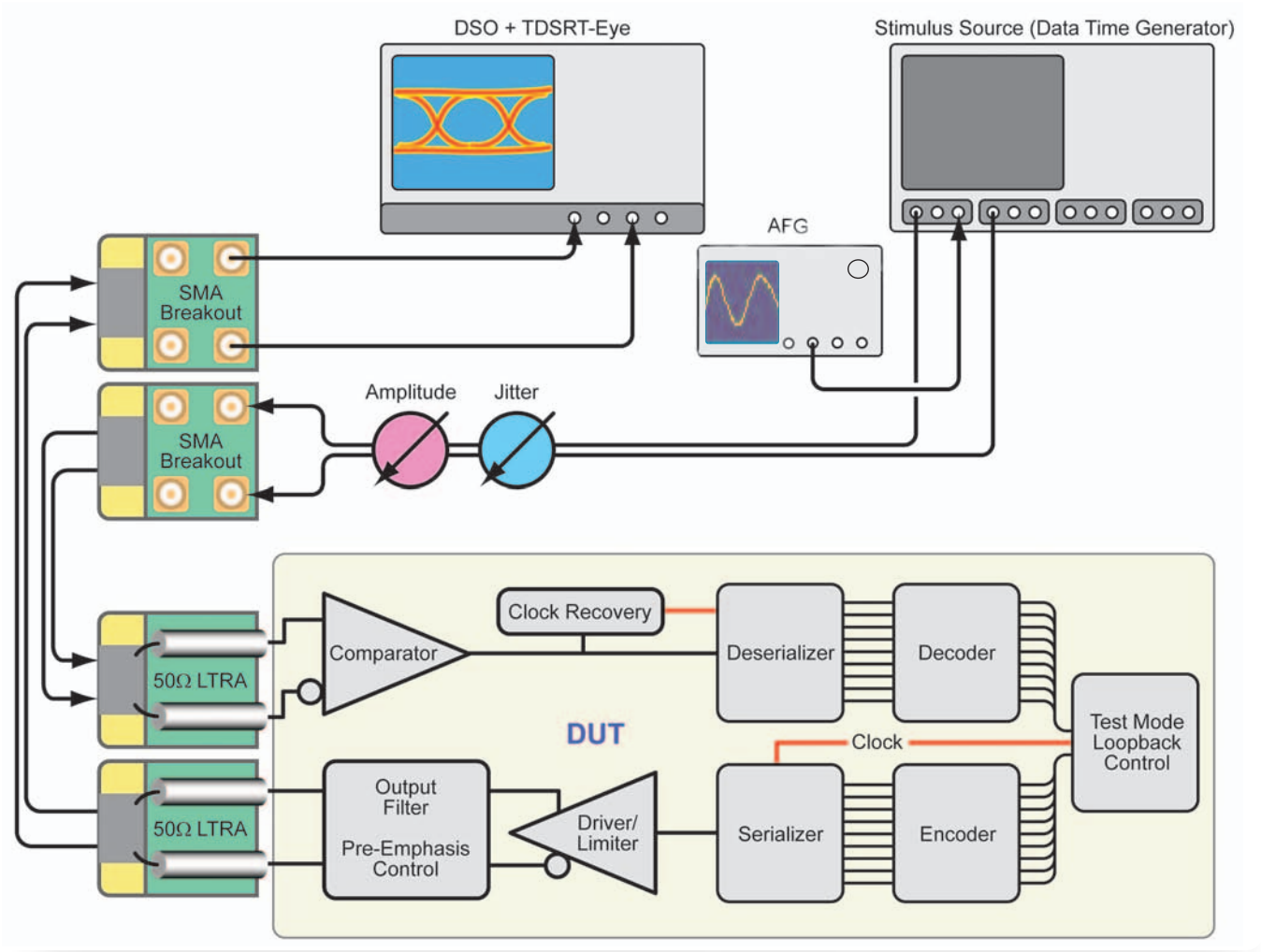


▶ **Figure 13.** *The de-emphasis signal produced by the data timng generator.*



▶ **Figure 14.** *DTGM31 Linear Jitter Output Module performance.*

Rigorous jitter tests are especially critical in applications such as PCI Express, in which the clock is embedded in the 8B/10B-encoded data stream. There is an absolute requirement for a signal source that can supply jitter with specific amplitude and frequency modulation characteristics.

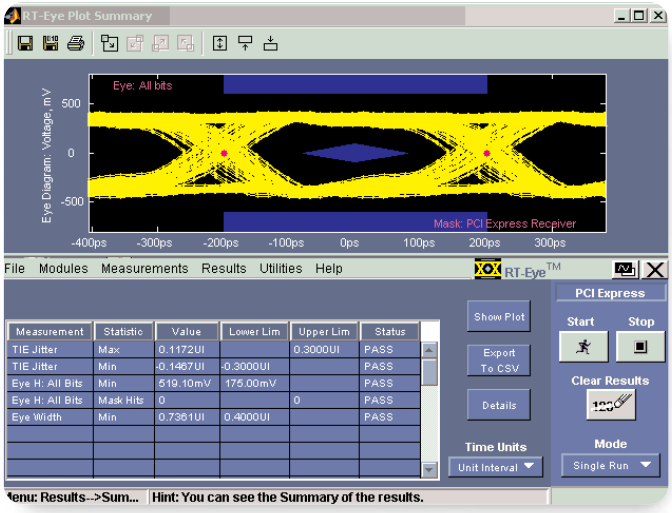


▶ **Figure 15.** *A jitter test system configuration for a PCI Express device.*

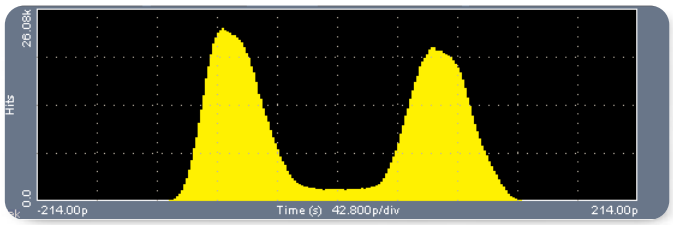
The DTG5000 Series includes sources with these important features. The DTG5000 Series instruments include a built in jitter and noise generator. The jitter generator can accept diverse modulation profiles such as sine, square, triangle and noise, and can be set to apply jitter to the rising or falling edge, or both. The maximum jitter frequency available in the standard DTG5000 Series models is 1.56 MHz.

The DTGM31 output module with a jitter modulation input makes it possible to generate jitter at higher amplitudes and frequencies when necessary. This DTGM31 delivers jitter at amplitudes up to 240 ps (peak to peak) at frequencies to 200 MHz using a 1V input amplitude from the source generator. Even higher jitter frequencies – up to 400 Mhz – can be modulated by increasing the input amplitude of the modulation source. Figure 14 shows a plot of DTGM31 input amplitude vs. jitter amplitude.

An external generator such as a function generator provides the jitter or noise modulation profile. The test system layout is shown in Figure 15.



▶ **Figure 16.** *TDSRT-Eye eye diagram summary screen.*

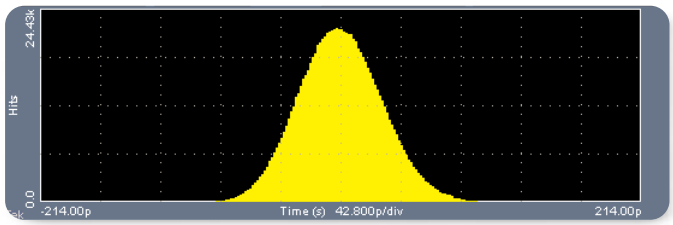


▶ **Figure 17.** *Jitter profiles resulting from a square wave input.*

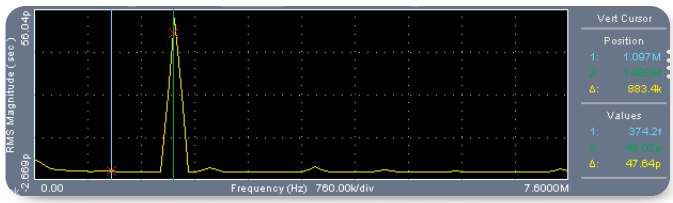
The PCI Express Base Specification, to cite an example, specifies jitter as the variation of the eye diagram crossing points relative to a recovered TX Unit Interval (UI). The DTG5334 or DTG5274 plus the DTGM31 module provide control of jitter in terms of both amplitude and frequency content. With this combination, thorough jitter tolerance testing of PCI Express receivers can be accomplished. Figure 16 is a results screen from a TDSRT-Eye[7] measurement on a 2 MHz jittered PCI Express eye. Figures 17 & 18 show the jitter profiles resulting from a square wave and Gaussian noise input, respectively, measured with TDSJIT3. Fig 19 shows a spectral display of the jittered profile using TDSJIT3.

A Jitter Tolerance Test Method

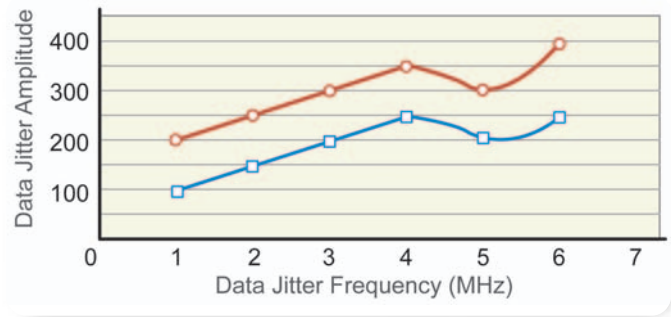
When designing and testing PLL circuits as part of a SERDES device, it is good practice to verify the jitter



▶ **Figure 18.** *Jitter resulting from a Gaussian noise input.*



▶ **Figure 19.** *Spectral display of the 2 MHz jittered signal.*



▶ **Figure 20.** *Jitter tolerance plot.*

tolerance at multiple frequencies. There are three steps to this process:

– Configure the SERDES in a loop-back mode, feed a clock or data into the serial data input port, and measure the serial output port with a jitter measurement tool. The Tektronix TDSJIT3 v2.0 jitter analysis software package for TDS Series oscilloscopes is ideal for this purpose. Adjust the jitter frequency across the range of interest and compare the jitter transfer between the input and output.

– Plot the results. Figure 20 shows a typical jitter tolerance plot

[7] TDSRT-Eye is an automated eye diagram measurement software package; TDSJIT3 v2.0 is an automated jitter measurement and analysis package. Both can be installed on Tektronix TDS Series oscilloscopes.

Standard	Data Rate	Reach	Condition	Jitter (UI)	Jitter Freq	Jitter Amp (ps-pp)
SATA1	1.5	Gen1i Gen1m	TJ at Connector, Data-Data, 5UI	0.43	None	287
		Gen1i Gen1m	DJ at Connector, Data-Data, 5UI	0.25	None	167
		Gen1i Gen1m	TJ at Connector, Data-Data, 250UI	0.6	None	400
		Gen1i Gen1m	DJ at Connector, Data-Data, 250UI	0.35	None	233
		Gen1x	TJ after CIC, Clk-Data, fBAUB / 1667	0.65	894kHz	433
		Gen1x	DJ after CIC, Clk-Data, fBAUB / 1667	0.35	894kHz	233
SATA2	3	Gen2i Gen2m	TJ at Connector, Data-Data, fBAUD / 10	0.46	300MHz	153
		Gen2i Gen2m	DJ at Connector, Data-Data, fBAUD / 10	0.35	300MHz	117
		Gen2i Gen2m	TJ at Connector, Data-Data, fBAUD / 500	0.6	6MHz	200
		Gen2i Gen2m	DJ at Connector, Data-Data, fBAUD / 500	0.42	6MHz	140
		Gen2x	TJ after CIC, Clk-Data, fBAUD / 1667	0.65	1.80MHz	217
		Gen2x	DJ after CIC, Clk-Data, fBAUD / 1667	0.35	1.80MHz	117

▶ **Table 2.** *Jitter tolerance requirements for SATA Gen I and II and PCI Express compliance.*

Using TDSJIT3 v2.0, it is possible to directly measure the magnitude of the jitter transfer function through a device. To do so, simultaneously probe the input and output of the device and set up similar measurements (i.e. Data Period measurements) at both points, then acquire and measure the jitter at each point.

Table 2 summarizes the jitter tolerances in three of today's leading standards, namely, Serial ATA, Serial ATA Gen II, and PCI-Express. The table exemplifies the oscilloscope of jitter testing defined in many serial standards.

Standard-Specific Tests

There are some tests worth noting that apply only to specific standards.

SATA Out-Of-Band Measurements (OOB)

Out-of-band signals are used for handshake signaling between an SATA device and its host. The OOB signals also ensure that Gen I receivers interoperate with Gen II transmitters. There are three OOB signals: COMRESET, COMINIT and COMWAKE.

Signaling is implemented as a burst of ALIGN primitives, or as a burst of D words composed of four D10.2 characters with a duration of 160 UI. The COMRESET signaling originates from a host controller and forces a hard reset in the connected device. The COMRESET signal must consist of at least six data bursts. COMINIT, a request for communication initialization, always originates from the device (a hard disk drive). COMINIT is electrically identical to the COMRESET signal. COMWAKE may originate from the host controller or the connected device. It is a transmission consisting of six bursts of data separated by an idle bus condition. The signal must contain no less than six data bursts.

An arbitrary waveform generator or a data timing generator (DTG) can be used for Out-Of-Band measurements. The instrument enables the host controller by emulating a device. The AWG/DTG must of course deliver a sample rate compatible with the data rate of the SATA device under test.

– For SATA Gen I, the AWG or DTG must have a sample rate of at least 1.5 GS/s. The Tektronix AWG615 and DTG5274 are suitable solutions for SATA Gen I.

– For SATA Gen II, the instrument's sample rate must be at least 3 GS/s. The Tektronix AWG710B and DTG5334 models can address these higher rates as well as those of SATA Gen I.

Some host devices may be unable to produce the ALIGN patterns specified for the OOB tests. In these situations, the AWG or DTG can be programmed to provide the necessary patterns for general performance analysis of both the host and the connected device.

Ethernet Return Loss Measurements

For Ethernet testing, return loss measurements are a critical measurement challenge. The measurements are a required part of the compliance test procedure. The return loss test provides an indication of the performance of the transmission system.

Return loss describes the degree of mismatch between a load and the characteristic impedance of the transmission system driving that load, summarized in Equation 2.

$$\mathrm{Re}\,turnLoss = \left(\left| 20 \log \frac{V_r}{Vi} \right| \right)$$

Equation 2: Return loss

Where Vi is the forward incident voltage a chosen point in the transmission channel and Vr is the reflected voltage at that same point.

If, for example the load is a short circuit, 100% of the voltage is reflected—a return loss of zero. The same is true if the load is an open circuit. If the load is exactly equal to the characteristic impedance, the reflected voltage is zero—a return loss value of minus infinity.

In a return loss measurement, a pre-defined waveform supplied by an AWG simulates the return loss of the device under test. The standard specifies the minimum amount of attenuation the reflected signal should have relative to the incident signal. A TDS7000B Series oscilloscope running TDSET3 Ethernet Compliance Test software performs the measurement automatically. This configuration eliminates the need for costly network analyzers that have traditionally done the job.

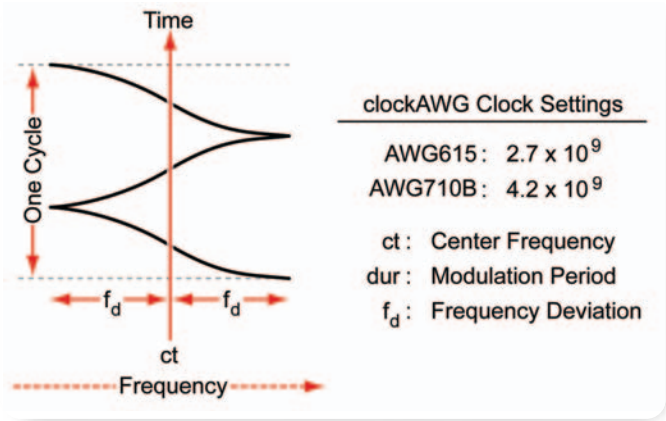
Spread Spectrum Clocking (SSC) Tests

Spread-spectrum clocking is an effective way to minimize radiated EMI from clock sources in high-speed systems. Increasingly, serial standards are implementing SSC, with the result that SSC has become a compliance issue.

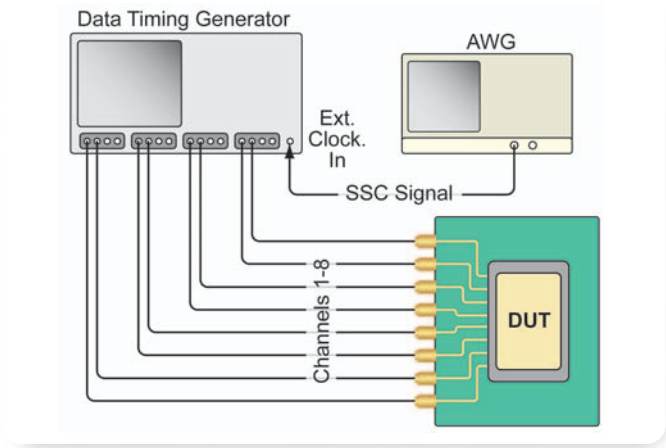
While generating a compliant SSC signal can be a challenge, it is within the capability of advanced arbitrary waveform generators such as the Tektronix AWG615 or AWG710B. These tools include powerful equation editing features that simplify writing SCC algorithms. Figure 21 is an SSC equation that illustrates this, while Figure 22 illustrates the resulting frequency behavior.

```
clock = 1e9    '@ Clock setting
ct = 100e6     '@ Center frequency
dur = 15e-6    '@ Duration per sweep cycle
fd = 0.625e6   '@ Frequency-to-frequency amplitude
alp = 1.0      '@ Correction

fm = 1/dur     ' Frequency for a sweep cycle

a1 = 0.000704          ' Equation parameters
a2 = 0  ' aX^3 + bX^2 + cX + d
a3 = 0.0441
a4 = 0

of = 7.5          ' Time offset
tunit = 30/dur  ' Time base for equation

'
' Coefficient for integration
'
yt = a1*of^3+a2*of^2+a3*of+a4
iyt = (a1*of^4)/4+(a2*of^3)/3+(a3*of^2)/2+(a4*of)
cff = iyt/yt/of
'
' Time - Frequency Characteristic
'
size = dur * clock / 2
"SSC1-":cf:"B.wfm" = a1*(time*tunit-of)^3 +
                     a2*(time*tunit-of)^2 +
                     a3*(time*tunit-of) + a4

"temp001.wfm" =  -1 * "SSC1-":cf:"B.wfm"
"SSC1-":cf:"B.wfm" = join("SSC1-":cf:"B.wfm","temp001.wfm")
"SSC1-":cf:"F.wfm" = integ("SSC1-":cf:"B.wfm")
"SSC1-":cf:"F.wfm" = norm("SSC1-":cf:"F.wfm")
"SSC1-":cf:"F.wfm" = "SSC1-":cf:"F.wfm" * alp * cff / 4 / fm
delete("temp001.wfm")

'
' Spread Spectrum Clock
'

"SSC1-":cf:"S.wfm" =
      sin(2*pi*(ct*time + fd*"SSC1-":cf:"F.wfm") - pi/2)
```

▶ **Figure 21.** *Equation for generating a compliant SSC signal.*



▶ **Figure 22.** *Characteristics of the SSC signal.*

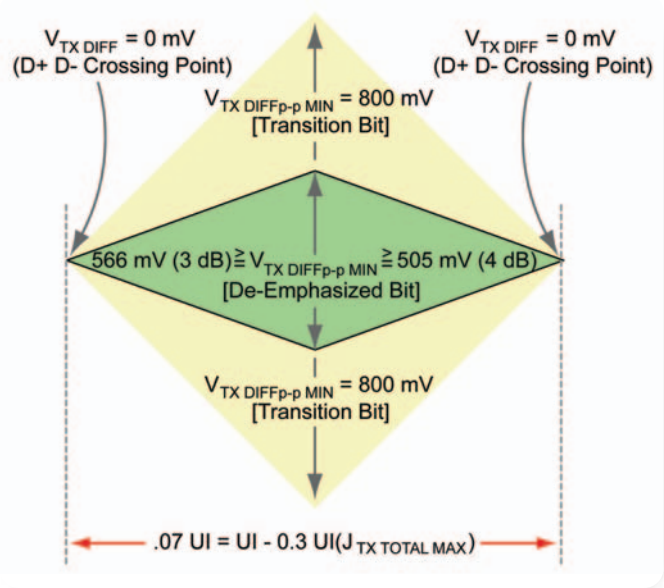


▶ **Figure 23.** *Using an AWG to drive a DTG5334 Data Timing Generator, which in turn produces multiple synchronized outputs.*

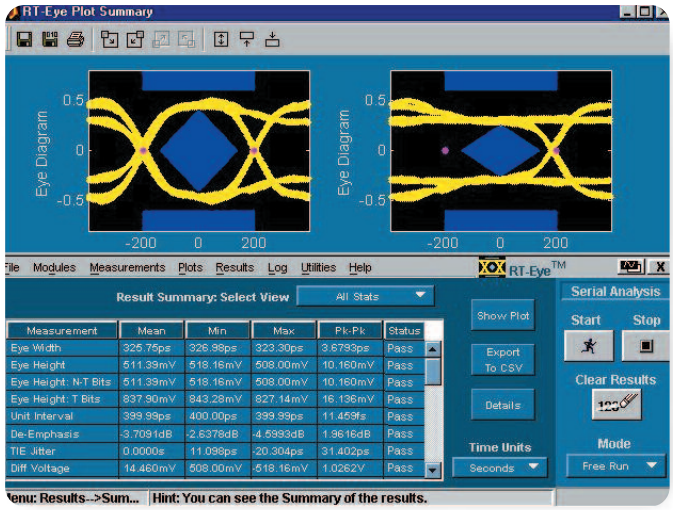
Using the equation (after compiling it), the AWG615 or AWG710B can be used as the clock source directly, or it may be fed into a DTG5000 Series instrument's external clock input to generate multiple outputs as shown in Figure 23.

Tx Measurements

Transmitter measurements rely heavily on eye diagrams captured with an oscilloscope of appropriate bandwidth and features (see sidebar, "An Acquisition And Analysis System For Serial Measurements"). Amplitude, jitter and timing results can be gleaned from just a few "eye" displays.



▶ **Figure 24.** *Transmit Waveform Mask defining minimum transmitter timing and voltage compliance specifications. (Source: PCI Express Base Specification - Rev. 1.0a).*



▶ **Figure 25.** *PCI Express Compliance Test using RT-Eye software.*

Eye Diagram Requirements

There are three waveform masks called out in the PCI Express Base Specification, two for the transmitter and one for the receiver. Additional test points for system and add-in cards (tested at the PCI Express connector) are called out in the PCI Express Electromechanical Specification. The transmit eye specification defines two differing amplitudes. De-emphasis is used in PCI Express to ensure the best eye opening with minimal Inter-symbol Interference (ISI) when transmitted through various lengths of FR4. The de-emphasis specification at the transmitter is 3.5 dB. The resulting waveform mask is shown in Figure 24.

The TDS6154C Oscilloscope waveform acquisition provides a sample rate of 40GS/s on all four channels. This provides actual waveform sample points at 25 ps/pt. After the data is acquired, it can be processed using Tektronix' TDSRT-Eye (Real-Time Eye) rendering technique. A typical TDSRT-Eye results screen is shown in Figure 25.

As described in section 4.3 of version 1.0a of the PCI Express Base specification, eye diagram mask testing must be performed by recovering the clock from the mean of 3500 consecutive bits. Within the 3500-bit clock recovery window, a 250-bit analysis window is defined, in which all mask testing and measurements are made. Once the clock is recovered from the waveform data, the transition bits and non-transition bits can be separated and mask testing can be performed as shown in Figure 25.

There are three key advantages of the TDSRT-Eye rendering technique when compared to traditional Equivalent Time (ET) methods. An ET-based measurement uses hardware clock recovery and builds the waveform with a series of acquisitions. Each acquisition is the result of one trigger event. Over time, the jitter-related error in this sequence of samples can accumulate. In contrast, the TDSRT-Eye method captures all the needed waveform data with one trigger event and one acquisition. Consequently the Jitter Noise Floor (JNF) is very small: approximately 750fs RMS when using a TDS6804B oscilloscope.

Secondly, TDSRT-Eye recovers the embedded clock from the waveform data using software DSP (Digital Signal Processing). This allows different clock recovery models to be used. In the case of PCI Express, two clock recovery techniques are used in the analysis. The clock is recovered from the mean of 3500 consecutive bits. Then the edges of the eye diagram are positioned with respect to the median of the clock within the 250-bit window. This is only one example. The TDSRT-Eye software also supports standard and custom PLL clock recovery methods as required by Rev. 1.1 of the base specification.

Lastly, because the waveform data is in acquisition memory, the data can be analyzed to determine which bits are transition bits and which are non-transition bits. These bits can be separated and compared to their respective masks. The TDSRT-Eye software compares the waveform with the mask and reports any mask collisions as failed bits

With an eye diagram many of the specific tests can be accomplished. Tests such as Amplitude, Jitter and Timing can all be measured using an eye diagram.

An Acquisition and Analysis System for Serial Measurements

Transmitter testing is the domain of the oscilloscope. As with the signal sources used in receiver testing, there are some key considerations when choosing an oscilloscope for Tx measurements. Among these are bandwidth, sample rate, probing capabilities, clock recovery features, and automation. When properly equipped, a modern DSO or DPO is a powerful solution.

Choosing the Right Oscilloscope

Oscilloscope system bandwidth and rise time performance must be given special attention when choosing a compliance measurement solution. The bandwidth of the oscilloscope should be three to five times the highest frequency of the target DUT. This protects against signal degradation in the analog domain (ensuring more accurate measurements throughout), and also supports quantitative measurements of amplitude and other parameters.

Risetime specifications, too, must be considered. Not all acquisition systems are created equal. An accepted definition that equates bandwidth and risetime (Equation 3) applies to a single-pole response. As instrument bandwidth increases, risetime typically decreases, which supports more accurate timing measurements and eye diagrams.

$$BW = \frac{0.35}{Risetime}$$

Equation 3: Oscilloscope risetime and bandwidth response.

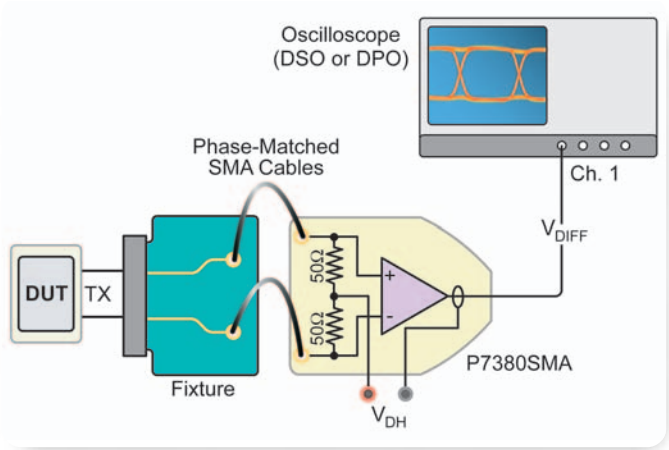
Most serial bus specifications specify risetime from "20-to-80%." This is the time it takes the signal to pass from 20% to 80% of its total amplitude swing. In the case of a 1-volt (1000 mV) total amplitude range, this would encompass the time it takes the signal to go from 200 mV to 800 mV.

It is important to understand that risetime specifications may be qualified as either 10-to-90% values or 20-to-80% values. Both contexts are valid. But predictably, the 20-to-80% values look better on paper, since the goal is to achieve the lowest possible risetime figure. But an instrument that delivers a 100 ps risetime, 10-to-90%, has effectively the same performance as one that claims a 70 ps risetime, 20-to-80%. The conversion factor (multiplier) is 1.4.

Circuit Board and Interconnect Testing Using True Differential TDR

An LVDS signal running at multi-gigabit data rates through a low-cost medium such as FR4 poses many layout challenges. In all high speed signaling technologies, board layout and interconnect characterization are critical to good signal integrity. The CSA/TDS8200 Series Oscilloscope with the 80E04 TDR sampling module delivers true differential TDR measurements on PCB traces, connectors, and cables. These measurements are required in order to understand the transmission characteristics of differential lanes used in today's serial buses.

Most cable and connector test requirements include impedance measurements that can be accomplished with TDR and TDT instruments. Another important cable test is the eye diagram in which a specific pattern such as a CJTPAT pattern from a DTG5000 Series drives one end of the cable. Then the eye is measured at the other end to determine how much degradation has accrued.



▶ **Figure 26.** *The P7380SMA probe captures differential signals using one oscilloscope channel.*

Automation

As this document has demonstrated, there are many tests required to ensure quality and interoperability in any new serial device. It is an application tailor-made for automated measurements, since the tests are repetitive, complex, and potentially time-consuming.

Probing Considerations for Transmitter Measurements

Test procedures including those defined for PCI Express assume that the transmit/receive link will be broken and terminated in a 100 Ω differential load (50 Ω per side). When the transmit SERDES driver sends out a training sequence and does not receive a response, the device concludes that it is transmitting to a piece of test equipment and begins to transmit a repeating compliance test pattern. Given the architecture, three different probing strategies are recommended for driver (or transmitter) testing.

The first option is to use two TekConnect TCA-SMA adapters (one on Ch1 and one on Ch3) on the TDS6000B Series oscilloscopes. The differential signal is defined by the math waveform (Ch1-Ch3). This is known as pseudo-differential acquisition. The advantage of this technique is that it takes full advantage of the bandwidth of the oscilloscope. The disadvantage is that the two channels must be de-skewed each time you set up the measurement to insure accurate timing measurements.

The second option is to provide a "dummy" load in a termination block and use the P7380 Differential Active Probe. Since this is a true differential probe, channel de-skew is not required.

The final option is to use the P7380SMA probe. The P7380SMA offers a true differential input fitted with SMA connectors. The probe's 8 GHz active architecture delivers the signal to one oscilloscope channel, eliminating the need for channel deskew. A block diagram (not to scale) is shown in Figure 26. The P7380SMA also includes a calibrated system which eliminates cable loss in the measurement.

Tektronix works closely with industry groups developing serial specifications. As each new standard (and its test requirement) emerges, Tektronix concurrently develops automated applications for its instruments. In some cases these instruments and applications themselves become a recommended part of the compliance procedure. The OpenChoice software environment of Tektronix TDS Family oscilloscopes enables users to control commercial and proprietary analysis tools as well as Tektronix application-specific software packages including:

– TDSUSB2 USB2.0 compliance package

– TDSET3 Ethernet compliance package

– TDSRT-Eye Serial Bus measurement package (with available application-specific modules for PCI Express and InfiniBand)

– TDSJIT3 Advanced Jitter measurement and analysis package

– Serial ATA Test signal quality measurement package

– TDSHT3 HDMI compliance test package

– TDSDVI DVI compliance test package

With many of these applications the oscilloscope can control other equipment such as AWGs and DTGs. The automation package set up the equipment required for each specific test. This minimizes the possibility of operator error and expedites the whole testing process.

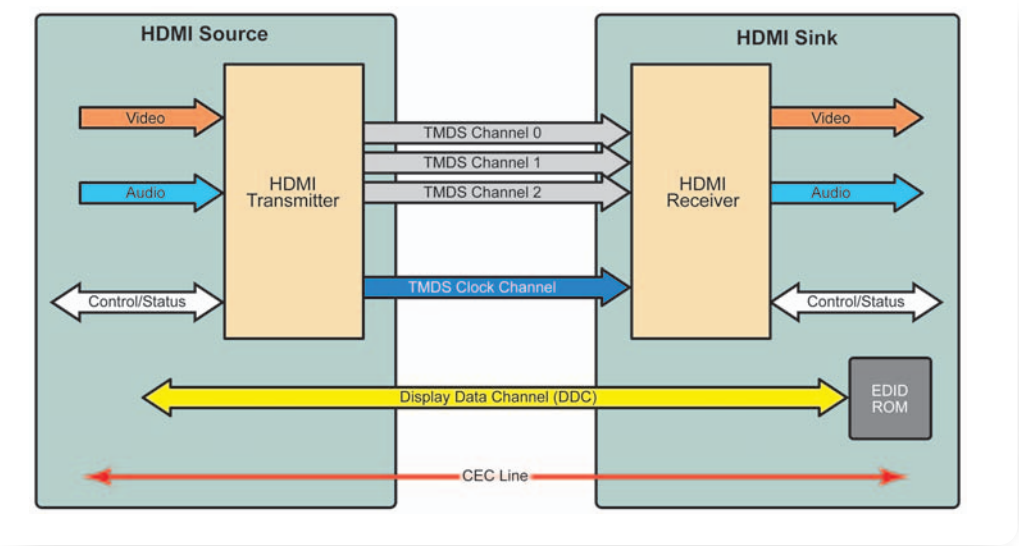
Conclusion

Serial data transmission using industry-standard buses such as PCI Express and Serial ATA are the way of the future. Serial devices bring with them a host of benefits as well as some challenges. Data rates are much higher than earlier parallel architectures; signaling requirements are more stringent. Every designer must understand, and find solutions for, serial measurement challenges.

This primer has examined issues such as basic serial signaling, SERDES architecture, transmitter requirements, and particularly the challenges associated with receiver testing. Serial transmitter testing is purely a matter of acquiring and analyzing signals produced by the device under test. But receiver testing requires stimulus sources including arbitrary waveform generators and data timing generators. Configuring and programming these sources to supply not only raw data but also characteristics such as jitter and de-emphasis is a major part of the designer's compliance testing task.

Proven tools such as the Tektronix DTG5000 Series Data Timing Generator make the task easier than ever before. Pre-written patterns, advanced editing features, and versatile modular output configurations allow the instrument to adapt to a broad range of serial test requirements. Acquisition tools such as the Tektronix TDS Family of oscilloscopes further simplify the engineer's compliance work with automated testing packages that include setup, analysis, and reporting features.

Appendix A



▶ **Figure S1.** *HDMI pixel data flow and organization from Source to Sink.*

Serial Architectures for Multimedia

In keeping with their application environment, which differs dramatically from that of computing-oriented buses, DVI and HDMI multimedia technologies take a different approach to signal transmission. Both use a high-speed serial interface based on transition-minimized differential signaling (TMDS) to send data to the receiver.

TMDS Signal Encoding

TMDS signals switch between "on" and "off" states using an algorithm that minimizes the number of transitions to avoid excessive levels of electromagnetic interference (EMI) on the cable. The differential signal amplitude is +3.3 volts, terminated in 50 Ω with 500 mV nominal amplitude transitions (from +2.8 V to +3.3 V).

The basic TMDS transmission line is made up of three data channels and a clock channel. Data consists of 8-bit pixels (256 discrete levels) in each of three channels (R/G/B). These are encoded into ten-bit words using 8B/10B encoding to minimize transitions and to remove the DC component. The signals have rise times on the order of 100 picoseconds. A pair of TMDS lines is used when higher data rates are needed. Figure S1 shows the flow of pixel data from a graphics controller or Source device to the digital Sink receiver.

Standard	Display Resolution	Data Rate	Clock Frequency
VGA	640 x 480	252 Mb/s	25.2 MHz
SVGA	800 x 600	400 Mb/s	40 MHz
XGA	1024 x 768	650 Mb/s	65 MHz
SXGA	1280 x 1024	1080 Mb/s	108 MHz
UXGA	1600 x 1200	1620 Mb/s	162 MHz
640 x 480p	640 x 480	252 Mb/s	25.2 MHz
720 x 480p	720 x 480	270.27 Mb/s	27.027 MHz
576p	768 x 576	270 Mb/s	27 MHz
720p	1280 x 720	742.5 Mb/s	74.25 MHz
1080i	1920 x 1080	742.5 Mb/s	74.25 MHz

▶ **Table S1.** *Standards and respective data rates.*

TMDS data rates range from 22.5 megapixels per second (Mpps) to 165Mpps, equivalent to or up to 1.65 G bits per second at the maximum clock rate of 165 MHz. The data rate depends on the display resolution. The relationships of display resolution, bit rate and clock frequency are shown in the Table S1.

HDMI Jitter Tolerance Testing

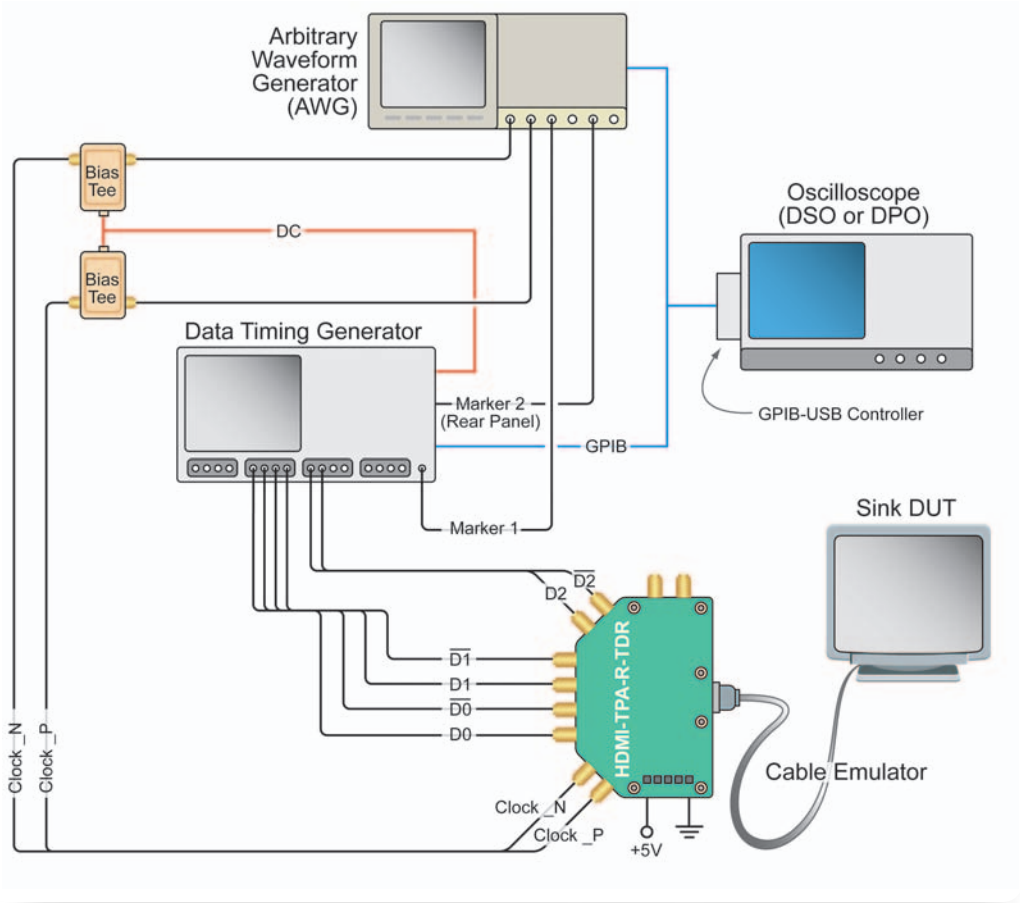
Jitter tolerance tests for HDMI require more strenuous jitter generation than their counterparts among serial buses for computing. For compliance, HDMI requires inserting two components of jitter to the clock signal. The DTG5000 Series instruments are fully compatible with either of two recommended jitter solutions. One solution pairs the DTG5000 Series generator with an arbitrary waveform generator for either compliance or characterization work; the other, lower-cost solution involves a jitter generator module plugged into the DTG5000 Series mainframe and driven by an external function generator. Both approaches provide the necessary modulated jitter profiles for the generated clock signal as follows:

– Arbitrary Waveform Generator (AWG) Method: This solution taps the full power of the DSO and its TDSHT3 application software, the DTG5000 Series instrument, and the AWG.

  The TDSHT3 software generates the specific jitter modulation waveform and sends it to the AWG710B, which in turn acts as the clock source for the jitter tolerance test. The jitter is steadily increased by the software until the device fails. The data lines are then verified by the oscilloscope for compliance.

The AWG has two digital "Marker" outputs that can be used for synchronization, among other purposes. In HDMI sink testing, one marker connects to the DTG5000 Series external clock input while the second marker connects to the DTG5000 Series trigger input, both providing synchronization. Data signals for the device under test are sourced by the DTG5000 Series. Bias Tees are required to bring the AWG710B output's clock signals up to the required TMDS levels. Conveniently, these Bias Tees can be powered by the built-in DC output on the DTG5000 Series. The AWG method is able to stress the device beyond the compliance specification levels, making it suitable for characterization work. Figure S2 illustrates the layout of a test configuration using the AWG method.

– DTGM32 and Function Generator Method: This approach is ideal for quick verification and cost-effective pre-compliance testing. The method uses a DTGM32 module (Figure S3, similar to the DTGM31 except it has two inputs for jitter modulation) plugged into the DTG5000 Series mainframe, in con junction with a 2 channel function generator to add the required jitter content. Figure S4 depicts this scheme. The DTGM32 module allows jitter components to be added to its output. The jitter amplitude is controlled by the input amplitude of the jitter source, in this case a Tektronix AFG3102. An input level of 1 volt produces up to 2 ns peak-to-peak jitter. Figure S5 illustrates a jitter spectrum produced using this method with 1 Mhz and 7 Mhz added.



▶ **Figure S2.** *Sink jitter tolerance test setup using an AWG as the jitter source.*

▶ **Figure S3.** *DTGM32 Jitter Generation Module.*

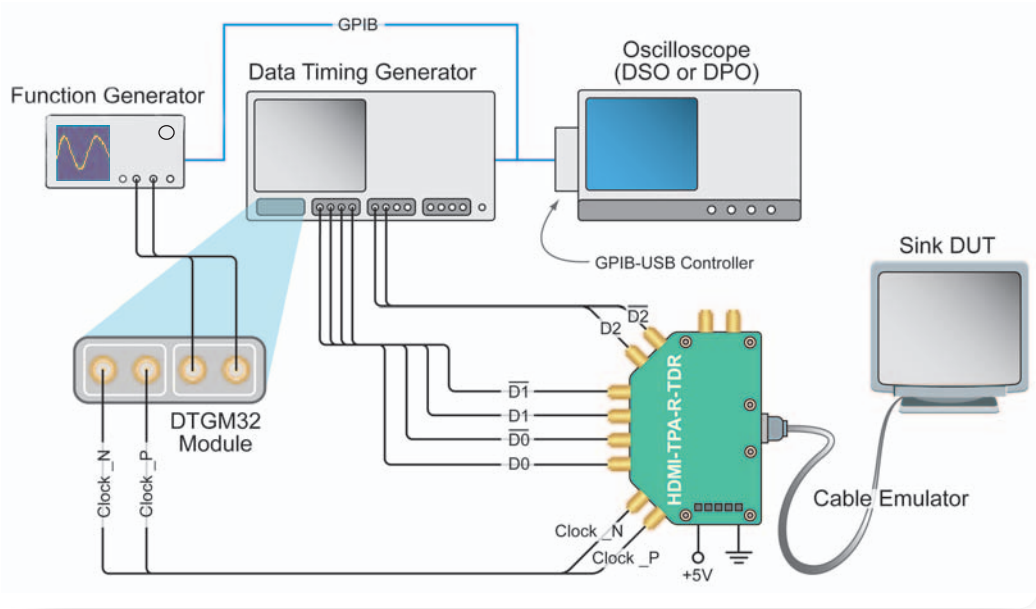


Figure S4. *Sink jitter tolerance test setup using a function generator to the jitter modulation source for the DTGM32 module.*

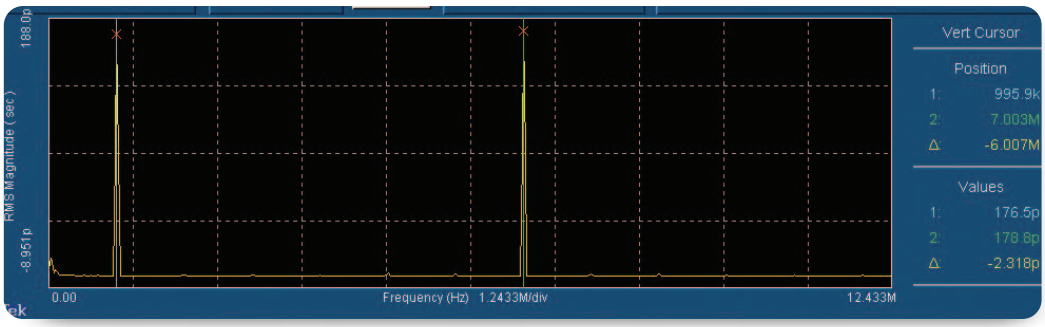


Figure S5. *Spectral display of jitter at 1 Mhz and 7 Mhz.*

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